IN THE CLAIMS

Please amend independent claim 1 as follows.

A clean version of the entire set of pending claims follows per 37 CFR § 1.121(c)(3). A marked-up copy of independent claim 1 as changed by this amendment, showing all changes made relative to the previous version of the independent claim 1, accompanies this paper on a separate sheet entitled "VERSION WITH MARKINGS TO SHOW CHANGES MADE" per 37 CFR § 1.121(c)(1)(ii).

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1. (Twice Amended) A data processing device, comprising

a register circuit for storing at least two addresses in parallel;

an address selector arranged to cycle through a set of states in which respective ones of the at least two addresses become a currently selected address respectively;

an instruction execution unit having an instruction set that contains a memory access instruction, execution of the memory access instruction causing the instruction execution unit to issue memory access signals with an access address determined from the currently selected address, execution of the memory access instruction further causing the address selector to cycle to a next one of the states; and

a control register that is instruction-settable to respective control states that control whether or not the processing device updates the at least two addresses as a side-effect of executing the memory access instruction.

2. The data processing device as claimed in claim 1, wherein each control state specifies respective update actions for all of the at least two addresses.

3. The data processing device as claimed in claim 1, wherein the control states specify a choice from at least no-update, update by incrementing with a predetermined value and update by decrementing with the predetermined value.

4. The data processing device as claimed in claim 1, wherein the execution of said memory access instruction further causes the instruction execution unit to perform, upon the currently selected address, the update action that is specified by the control state of the control register for that one of the at least two addresses that is the currently selected address.

5. The data processing device as claimed in claim 1, wherein the instruction set includes a load from memory instruction and a store to memory instruction for causing the instruction execution unit to respond [as claimed for] to the execution of said memory access instruction

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8. The data processing device as claimed in claim 1, wherein the address selector cycles back and forth between states that select a first and second one of the at least two addresses respectively.

9. The data processing device as claimed in claim 1, wherein the register circuit stores at least three addresses, and the address selector cycles through a series of at least three states that select different ones of the at least two addresses.

10. A data processing device, comprising

a register circuit for storing at least two addresses in parallel;

an address selector including a register selector register and a logic circuit collectively arranged to cycle through a set of states in which respective ones of the at least two addresses become a currently selected address respectively;

an instruction execution unit having an instruction set that contains a memory access instruction, execution of the memory access instruction causing the instruction execution unit to issue memory access signals with an access address determined from the currently selected address, execution of the memory access instruction further causing the address selector to cycle to a next one of the states; and

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a control register in communication with said register selector register and said logic circuit, said control register being instruction-settable to respective control states that control whether or not the processing device updates the at least two addresses as a side-effect of executing the memory access instruction.